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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,628	12/14/2001	Timothy Calvin Visser	Smiths P177US	9214

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EXAMINER	
CHARIOUI, MOHAMED	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,628	VISSER ET AL.	
	Examiner	Art Unit	
	Mohamed Charioui	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 7** is objected to because of the following informalities: In page 6, line 3, change "a predefined level said external connecting pin" to --a predefined level to said external connecting pin--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is the step that shows how the faulty connection is restored.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Laing et al. (U.S. 5,399,975).

Laing et al. teach applying a voltage signal of a predefined level to the external connecting pin (see col. 2, line 57 to col. 3, line 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabele et al. (U.S. 5,991,521) in view of Laing et al. (U.S. 5,399,975).

As per claims 1 and 2, Gabele et al. teach using an integrated circuit programming device, executing a device read command (see col. 4, lines 4-45); obtaining an error message from the programming device identifying certain of the connecting pins appearing to be disconnected from a memory circuit element (see col. 4, lines 22-30).

Gabele et al. fails to teach applying a voltage signal to the certain of the connecting pins.

Laing et al. teach this feature (see col. 2, line 57 to col. 3, line 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Laing et al.'s teaching into Gabele et al.'s invention, because a voltage signal would be applied to the pins that are detected to have faulty connection. Therefore, current would flow through the pins to power up the elements connected by the pins to the rest of the circuit.

As per claims 3-6, Gabele et al. teach the system as stated above except that the step of applying comprises applying the signal to the certain connecting pins through a resistor.

Laing et al. teach this feature (see col. 2, line 57 to col. 3, line 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Laing et al.'s teaching into Gabele et al.'s invention, because the voltage would be applied to the pin through a resistor that would limit the current flowing through the pins. Therefore, system would not experience excess of current flow that might cause damage in the system.

Prior art

5. The prior art made record and not relied upon is considered pertinent to applicant's disclosure:

Hamblin ['862] discloses system for detecting faults in connections between integrated circuits and circuit board traces.

Intrater ['251] discloses apparatus and method for testing the connections between an integrated circuit and a printed circuit board.

Chehadi et al. ['931] disclose methods of operating an integrated circuit with memory having an internal circuit for the generation of programming high voltage.

Shiratori ['031] discloses method of testing interconnections of an LSI on a simulator through the use of effective pulse widths.

Druschel et al. ['294] disclose process and apparatus for individual pin repair in a dense array of connector pins of an electronic packaging structure.

Khazam et al. ['753] disclose simultaneous capacitive open-circuit testing.

Raymond et al. ['359] disclose method of detecting possibly electrically open connections between circuit nodes and pins connected to those nodes.

Aton et al. ['897] disclose method and apparatus for testing passive substrates for integrated circuit mounting.

Hsieh et al. ['824] disclose diagnostics of a board containing a plurality of hybrid electronic components.

Crook et al. ['209] disclose identification of pin-open faults by capacitive coupling through the integrated circuit package.

Keirn et al. ['451] disclose identification of pin-open faults by capacitive coupling.

Contact information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached Monday through Friday, from 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohamed Charioui

11/17/04

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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